

Low Cost Ferroelectric Loop Study Set up With New and Simple Compensation Circuit: Operated at Variable Frequencies

SADHAN CHANDRA DAS,¹ ABHIJIT MAJUMDAR,^{2,*}
AGA SHAHEE,¹ NIRANJAN P. LALLA,¹ T. SHRIPATHI,¹
AND RAINER HIPPLER²

¹UGC-DAE Consortium for Scientific Research, University Campus,
Khandwa Road, Indore 452001 (M.P), India

²Institute of Physics, Ernst-Moritz-Arndt-Universität Greifswald,
Felix-Hausdorff-Str. 6, 17489 Greifswald, Germany

(Received August 3, 2010; in final form April 5, 2011)

We report a cost effective high power (500 W) ferroelectric loop study set up. It has a new type of simple compensation circuit for continuous compensation of stray linear capacitance and large value resistive losses of the sample. It can be operated at continuous variable frequency modes to observe the loop structure at different frequencies. The proposed system has a drive voltage of 8400 V peak to peak and can be modified to higher voltage and higher frequencies. Instead of a loop plotter, it has a data saving facility for binary or ASCII files such that further processing of the data by computer software such as origin, excel etc can be achieved. This high power set up is suitable for a highly lossy sample. Moreover, uncompensated and compensated loop studies and time dependent loop growth observation for ceramic BaTiO₃ are discussed here in.

Introduction

In 1921, J. Valasek manually plotted ferroelectrics loops of Rochelle salt using a ballistic galvanometer and a dc voltage set up [1]. Later on Sawyer and Tower (1930) proposed a circuit for characterization of ferroelectric hysteresis loops [2] that were suitable for materials of low loss and high polarization. To this date the basic circuit configuration for measurement of ferroelectric loops is the same as that given by Sawyer Tower (S-T). In Fig. 1(a), we brush up and discuss fundamental phenomena such as spontaneous polarization, remnant polarization and coercive field for typical ferroelectric loops. Figure 1(b) shows the various compensation effects of a FE loop. After S-T it became obvious that a circuit that provided cancellation for resistive losses and stray capacitances was required, particularly for lossy samples. Diamant et al. (1957) [3] and Roetchi (1962) [4] described circuits, which compensate for finite conductivity of samples and linear stray capacitances of circuits. Sinha et al. (1965), described a circuit that compensates for finite conductivity of a lossy sample but not its stray capacitances [5]. Most of the applied electric fields are at

*Corresponding author. E-mail: majumdar@physik.uni-greifswald.de

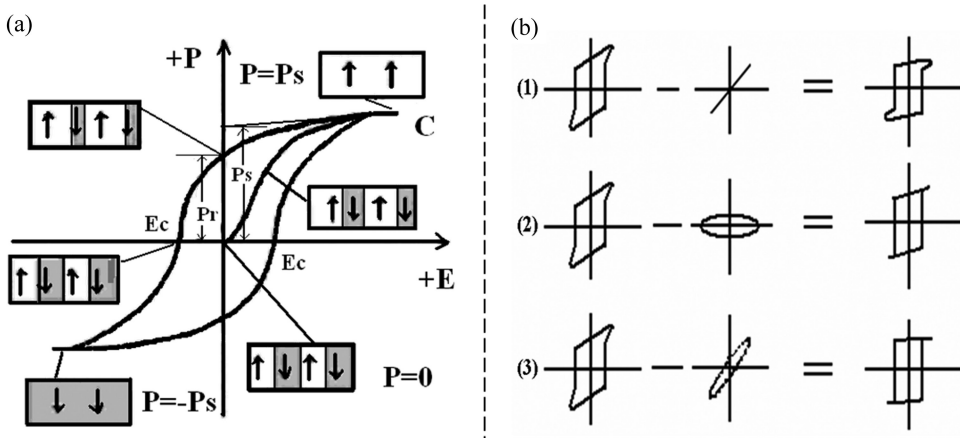


Figure 1. (a) A typical ferroelectrics loop where E_c = Coercive Field; P_r = Remnant Polarization and P_s = Spontaneous polarization. (b) Compensation of hysteresis loop for (1) linear stray capacitance only, (2) resistive losses only and (3) full Compensation of a hysteresis loop [3] provided sample has no linear part of capacitance.

a main frequency of 50/60 Hz and those circuits were not easy to fabricate in most research laboratories. Moreover, due to a lack of data saving facilities, loops had to be stressed from the oscilloscope screen. The data were neither stored nor plotted, hence could not be retrieved at a latest time. Glazer et al. (1983) overcome this difficulty by introducing a circuit that compensate for both resistive losses and stray capacitance with the facility of plotting the loops on a, xy plotter [6]. He applied the electric field over the frequency range from 0.1 Hz to 100 Hz with voltage ± 1 kV. Dias et al. (1994) developed an automated circuit and plotted the loops [7]. But both the above said circuits contain many components and cannot be constructed easily by the researcher. Moreover, costly commercial instruments are out of the reach of many physicists and researchers. In recent times, Meyer et al (2005) nicely described a measurement procedure to eliminate the leakage current on the basis of two ac current measurements performed at adjacent frequencies [8]. As the work was on a thin film, they had to use drive voltages in the range of a few voltages (± 6 V). So, from the above it is seen that after the S-T circuit a number of modified compensation circuit were developed and reported. Evaluation was towards simplicity of the circuit but the purpose was the same as that to compensate finite resistive losses and/or to compensate current due to the linear stray capacitances.

In this paper we report a simple ferroelectric loop study set up (Apparatus) with a new type of compensation circuit. The proposed set up has following advantages:

- (i) Its compensation circuit is simple and new because we generated the cancellation current both for resistive loss and capacitive compensation using a secondary tapped transformer (Fig. 2) which was very simple and novel. Here cancellation of those currents is done by the method of Kirchoff's current law.
- (ii) It can be easily fabricated, assembled, dismantled and repaired by any researcher and it works with continuous variable frequencies to observe loops at different frequencies. It has a data saving facility to store data and subsequently retrieve it for further processing by software.
- (iii) The system is of high power (500 W) so it can be used for highly lossy samples. Its high drive voltage (8400 V peak to peak) is suitable for thicker samples. Voltage

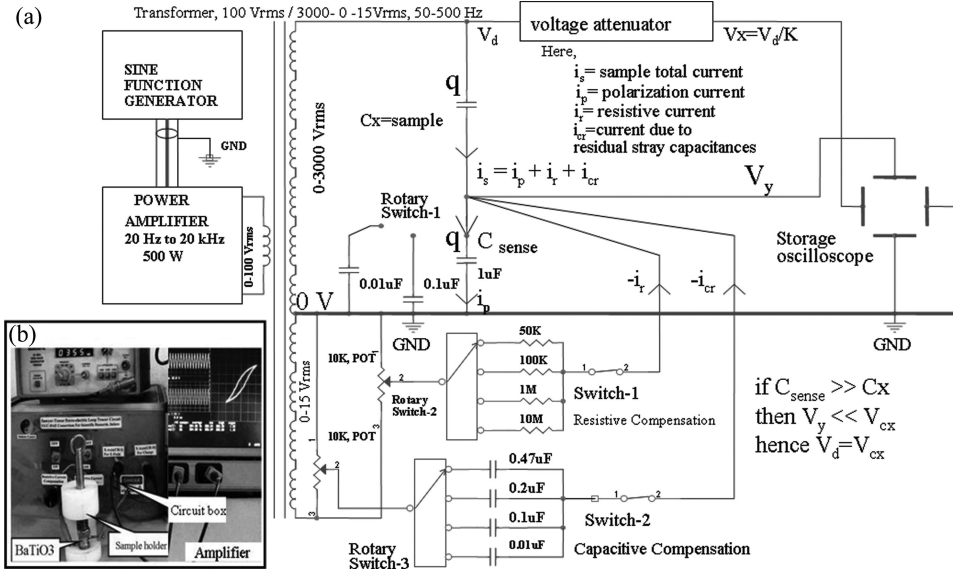


Figure 2. (Color online) Block diagram of ferroelectric loop tracer compensation circuit. In the insight below the developed compensation circuit equipment is indicated by the box. Teflon body sample holder, diameter of 50 mm. Parallel plates made of brass for sample holding have diameter of 15 mm.

amplitude control makes it useable for operation lower voltages hence to study thinner samples.

- (iv) The unit is modifiable to further higher voltages and frequencies just by changing to a transformer with suitable core material (ferrite core) and turns ratio. It is very low cost set up compared to commercially available systems and in this respect it is affordable by most researchers.

We present the data and photos of the loops taken at various frequencies that we presently mentioned.

II. APPARATUS

The schematic diagram of a ferroelectric loop tracer circuit is shown in Fig. 2. The ferroelectric loop tracer apparatus is an assembly of several components as follows:

- A. Spring loaded sample holder
- B. Electrical inputs
- C. Compensation circuit
- D. Spectrograph (Digital Storage oscilloscope)

A. Spring loaded sample holder

The body of the sample holder (insight of Fig. 2) is made of Teflon and it is home made. The parallel plates between which the sample is held are made of good quality brass. Their

faces are well polished. In actual experiment the holder is kept in oil so that it is immersed up to top level of the upper parallel plate to avoid discharge due to fringe field.

B. Electrical Inputs

The electrical system is accompanied by (i) a high voltage transformer (8400V_{pk-pk}) which works from 50 to 500 Hz; (ii) function generator; (iii) power amplifier for inductive load (20 Hz to 20 kHz, 500 W); (iv) a resistive voltage divider for voltage measurement (1:21) and a (v) storage oscilloscope with a data saving facility (LeCroy Waverunner, dual channel 350 MHz, 1GS/s, LT262 model, DSO). The oil used here has a dielectric strength of 100kVrms/cm, a dielectric constant between 2.2 – 2.3, a maximum pour point –10 °C and a minimum flash point of 145 °C. The function generator (20 MHz, model no. HM5032) delivers a sinusoidal out put that is fed to a power amplifier with a 0–100 V_{rms} output voltage. The resistive voltage divider (1:21) circuit was made of resistances. Instead of a resistive divider one can use high a voltage oscilloscope probe (1:100).

C. Compensation Circuit

(i) *Circuit diagram and operation.* The developed set up can operate with a frequency range between 50–500 Hz sinusoidal signals. Here the secondary coil of the high voltage transformer is tapped to get 3000-0-15 volts RMS. So when the sign of instantaneous voltage with respect to tapped point of one terminal of the secondary coil is positive, then sign of the other terminal is negative. The tapped terminal is grounded. Thus the phase reversal (180°) is done with respect to ground potential. In the compensation circuit, the resistive net-work consists of 10 MΩ, 1 MΩ, 100 KΩ and 50 KΩ resistances and the capacitive net-work consists of 0.01 μF, 0.1 μF, 0.2 μF and 0.47 μF linear capacitors. In most cases, only a 10 MΩ resistor and a 0.1 μF capacitor are used and current magnitudes are varied by a potentiometer 10 KΩ in the compensation circuit. C_{sense} is a linear standard capacitor and its value can be chosen as 0.01 μF, 0.1 μF or 1 μF by a rotary switch. In most of the cases 1 μF is selected. The voltage (V_y) with respect to ground, which is developed across C_{sense} is applied to channel-2 of the oscilloscope and the drive voltage (V_d), after attenuation, is applied to channel-1. The X-Y mode of display is selected to see the loop and the data is then saved. The polarization (P) of the sample and the applied electric field (E) are calculated from the known area (A) and the thickness (d) of the sample. There are three instantaneous current components passing through the sample; the polarization current (i_p), the conductive current (i_r, if the sample is lossy) and the current due to linear stray capacitances (i_{Cr}). Their effects can be realized as per the Fig. 1(b). The latter two, i_r and i_{Cr}, contribute openness (i.e. rounded ends) and added inclination of the end parts of the P-E loop and these require compensation.

The described compensation circuit minimizes i_r and i_{Cr} by reversing the phases (180° shifts) of current i_r and i_{Cr} and adding them in suitable magnitudes to the junction of C_x and C_{sense} i.e. Kirchoff's current law. The phase shift due to resistive loss can be defined by $\tan\phi = (2\pi f r C_r)^{-1}$ [2]. So the effect of resistive current, i_r can also be minimized by increasing the frequency of the driving voltage only. From Fig. 3 we get, $q = q_{C_x} = q_{C_{sense}} = C_{sense} V_y$. So, Polarization (P) = q/A = (C_{sense}/A) V_y, is measured in μC/cm². The electric Field strength (E) = V_d/d, where 'd' is thickness in cm and is measured in Volts/cm. It is to be mentioned here that the current magnitudes for both resistive and capacitive compensation are varied by the 10 KΩ potentiometers in the compensation circuit as shown in Fig. 2.

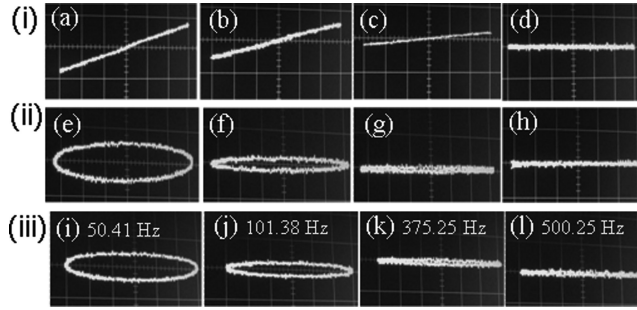


Figure 3. (color online) (i) Inclined straight lines due to linear capacitance in the place of sample (C_x). Frequency kept constant at 102.49 Hz; the change of inclination as follows, (a) the inclination at starting time of the measurement, (b & c) the inclination starts to decrease as the compensation capacitive current increases, (d) the maximum compensation observed. (ii) The loop due to resistive current at starting time of the measurement, (b & c) as the compensation current increases, the loop area starts to reduce and ultimately the maximum compensation observed in (d). (iii) At a constant load of 10 M Ω in the place of sample (C_x), the effect of resistive current compensation by increasing the frequency of the driving voltage where (a) at the initial stage of 50.41 Hz, (b) at 101.38 Hz, (c) at 375.25 Hz and the oval shaped loop is became a straight line at (d) 500.25 Hz.

(ii) *The working principle of compensation circuit.* We tested the circuit taking a resistance of 10 M Ω and capacitance of 1.4 nF in the place of sample (BaTiO₃) and compensated those values using our set up.

A. Realization of capacitive current (i_{cr}) compensation:

To realize the compensation of residual capacitive current, one linear capacitor of approximately 1.4 nF was connected in the place of sample (C_x). The driving voltage was increased (1200 V_{pk-pk}) and one inclined straight line was observed. The using only the capacitive compensation circuit, the current was gradually increased and we found that the inclination of the straight line was decreasing towards x-axis as shown in Fig. 3 (i). This way we can reduce the effect of residual capacitive current during the ferroelectric loop study. This capacitive compensation circuit is meant for compensation of circuit stray capacitance only not the linear part of the sample. Thus using suitable current selection we could successfully compensate 1.4 nF capacitance, though the stray capacitance is much lesser than this value.

B. Realization of Resistive current (i_r) compensation:

To realize the function of the resistive current compensation, one resistance of 10 M Ω was connected in the place of sample (C_x), the driving voltage was increased to a certain value (around 1200V_{pk-pk}) and found that one oval shape loop was developed due to phase shift. Now only using the resistive current compensation circuit, the current was gradually increased and it was seen that the loop gradually diminishes to a straight line along x-axis as shown in Fig. 3 (ii).

C. Realization of minimization of the effect of resistive current by increasing only the frequency of drive voltage:

The minimization of the effect of resistive current can be done by increasing only the frequency of the drive voltage. This could be realized by connecting the same 10 M Ω in

the place of the sample (C_x) and applying the voltage up to certain amplitude (around 1200 V_{pk-pk}). Then the frequency of the drive voltage was increased and we found that the oval shape of the loop diminished at 500 Hz and became a straight line as shown in Fig. 3 (iii). During this experiments both the resistive and capacitive compensation circuits were switched off by switches- 1 and 2 as shown in Fig. 2.

The explanation of the above can also be realized by the mathematical calculation of phase shift due to resistive path of the sample where phase angle ϕ can be represented by $\tan\phi = (2\pi f r C_r)^{-1}$ [2]. If we increase the frequency then the effect of phase angle reduces. If the sample is lossy, the total current i_s (Fig. 3) can be represented as:

$$i_s = i_p + i_{cr} + i_R$$

$$\text{Or, } \frac{dq}{dt} = \frac{dq_p}{dt} + \frac{dq_{cr}}{dt} + \frac{V_{ex}}{R}$$

$$\text{Or, } q(V_d) = q_p(V_d) + C_r \cdot V_d + \frac{1}{R} \int V_d dt$$

The first term describes the spontaneous polarization (compare Fig. 3). The second and third terms refer to the residual capacitance and the conductivity, respectively. Assuming $V_d = V_{cx} = V_0 \sin \omega t$, we get,

$$\text{Or, } q(V_d) = q_p(V_d) + C_r \cdot V_0 \sin \omega t + \frac{1}{R} \int V_0 \sin \omega t dt$$

$$\text{Or, } q(V_d) = q_p(V_d) + V_0 \frac{C_r}{\cos \phi} [\sin(\omega t - \phi)]$$

Where, $\cos \phi = \frac{C_r}{\sqrt{C_r^2 + (\frac{1}{\omega R})^2}}$ and $\tan \phi = \frac{1}{2\pi f RC}$

So, the 2nd and 3rd part of the equation is shifted and is displayed as a function of $V_0 \sin(\omega t - \phi)$. From the relation, $\tan \phi = \frac{1}{2\pi f RC}$, it is seen that if we increase the frequency the effect of resistive loss is minimised and the resulting loop will appear similar to that of a nonconducting sample [2].

III. Results and Discussion

The developed set up was first tested with a load of 10 M Ω resistance and 1.4 nF linear capacitance. Using the resistive compensation circuit we could compensate large value of resistive loss current, as shown in the Fig. 3 (ii); the oval shape becomes a straight line. Using the capacitive compensation circuit we could rotate the inclined linear straight line to the horizontal position as shown in Fig. 3 (i). It means if the circuit stray linear capacitance is 1.4 nF, then it can successfully be compensated using our circuit. But, practically the circuit stray linear capacitance is much less than 1.4 nF. We would also mention here that the linear capacitive compensation circuit is intended for compensation of the capacitive current of the linear stray circuit capacitance, not the linear part of the sample capacitance. The circuit was tested for minimizing the effect of resistive loss by increasing the frequencies by step by step as the result shown in Fig. 3 (iii). At 501 Hz the oval shape due to resistive current become a straight line.

Figure 4 (i) shows the uncompensated and compensated loops of BaTiO₃ sample of 0.039 cm thickness and 1.4 cm diameter. The optimized compensated PE loop was obtained at maximum electric field of 37.6 kV/cm and we found that the coercive field was $E_c =$

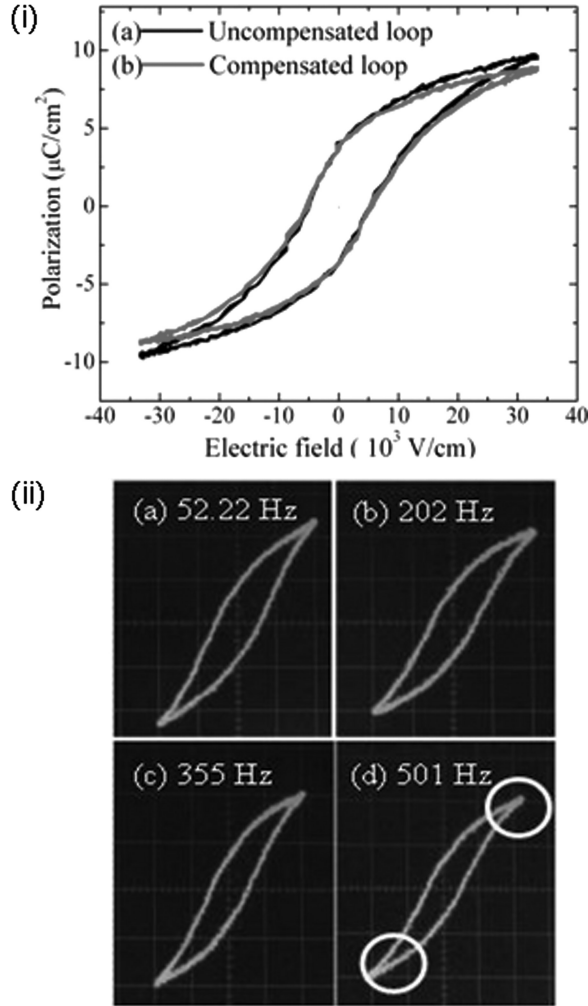


Figure 4. (i) Hysteresis loop of BaTiO₃ ($T = 0.039 \text{ cm}$, $D = 1.4 \text{ cm}$) using our developed set up (a) uncompensated loop, maximum electric field $33.6 \text{ kV}/\text{cm}$ and (b) compensated loop, maximum electric field $37.6 \text{ kV}/\text{cm}$. (ii) BaTiO₃ ferroelectric loop study with respect to the applied frequency (a) $f = 52 \text{ Hz}$, (b) $f = 220 \text{ Hz}$, (c) $f = 355 \text{ Hz}$ and (d) $f = 510 \text{ Hz}$. In case of (d) the openness of the loop end is reduced due to the elevated frequency and it has been marked by white circle.

$5.45 \text{ kV}/\text{cm}$, remnant polarization was $P_r = 3.65 \mu\text{C}/\text{cm}^2$ and spontaneous polarization was $P_s = 8.4 \mu\text{C}/\text{cm}^2$. We could not apply the electric field more than $38 \text{ kV}/\text{cm}$, because the sample breakdown took place at around the field of $38 \text{ kV}/\text{cm}$. Resistive compensation effect of BaTiO₃ sample can be realized from Fig. 4 (ii). As the frequency of the driving voltage is increased the openness of the ferroelectric loop reduced and marked by a circle (Fig. 4 (ii)). It is seen that at 501 Hz , the openness of the end parts of the ferroelectric loop of BaTiO₃ was reduced. The major factor of the openness is due the resistive loss and that has been reduced by increasing the frequency. In Fig. 3 (ii), we have used a constant load resistance of $10 \text{ M}\Omega$ for the resistive compensation to check the efficiency of our developed system where as in Fig. 4 (ii) we have used the BaTiO₃ sample to justify the same effect.

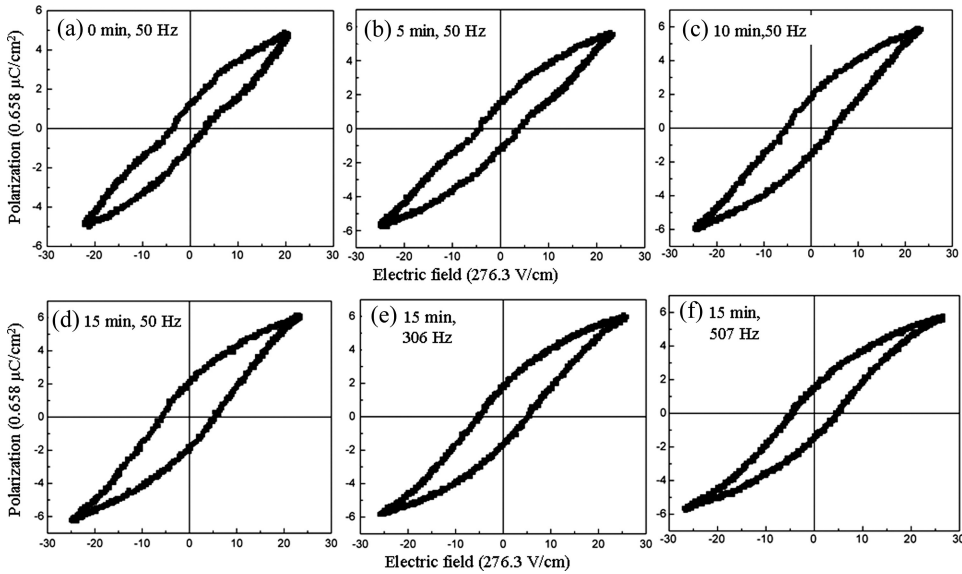


Figure 5. Time dependent growth of loops at 50 Hz where (a) just after the application of electric field (loop is propeller shape), (b) after 5 min, (c) after 10 min, (d) after 15 mins (loop became normal shape). Loops are at various frequencies (e) loop shape at 306 Hz (after the normal shape took place after 15 mins at 50 Hz), (f) loop shape at 507 Hz. Sample (BaTiO_3) used for this of thickness 0.076 cm and diameter of 1.39 cm. High electric fields have been not applied at present study.

In both cases we observed the same phenomena for the compensation. The full breakdown voltage has not been applied across the latest sample.

In the Fig. 5(a) it is seen that the loop looks like a propeller and in Fig. 5(b) and (c) the loop structure change after 5 mins and 10 mins. After 15 mins (Fig. 5d) it is seen that the loop has taken its normal shape. The loop just after the ac application was a propeller like hysteresis [9]. The propeller loop is caused by transverse internal fields due to pre-poled charges. With a small external voltage the spontaneous polarization is pinned by the internal field in its direction. With a large external voltage the spontaneous polarization is forced to turn in the direction of large applied field. The free charges homogeneously distributed with the successive application of high ac voltage to make the effect of internal field weak. The frequency was changed to 306 and 507 Hz after the normal shape of the loop occurred at 50 Hz. Data was collected as shown in the Fig. 5(e), (f). Here also it is seen that at higher frequency the effect of resistive loss is minimized.

IV. Summary

A low cost ferroelectric loop study set up with a new and simple compensation circuit working at variable frequencies (50–500 Hz) has been developed. The system can be modified for drive voltages up to 22 kV (peak to peak) and working the frequency range can be extended up to 20 kHz by using a suitable ferrite core transformer. The irreversible sample break down took place just above 38 kV/cm otherwise the field could be further developed up to 100 kV/cm for the same sample of 0.039 cm thickness and 1.4 cm diameter.

Acknowledgment

The authors acknowledge Dr. Praveen Chaddah (Director, CSR) and Prof. Ajay Gupta (Centre-Director, CSR) for their kind interest in FE loop tracer system. Part of this work was supported by the Deutsche Forschungsgemeinschaft (DFG) through SFB/TRR24 “Complex Plasmas”. Aga Shahee would like to acknowledg CSIR-India for financial support.

References

1. J. Valasek, *Phys Rev.* **17**, 475 (1921).
2. C. B. Sawyer and C. H. Tower, *Phys. Rev.* **35**, 269 (1930).
3. H. Diamant, K. Drenck, and R. Pepinsky, *Rev. Sci. Instrum.* **28**, 30 (1957).
4. H. Roetschi, *J. Sci. Instrum.* **39**, 152 (1962).
5. J. K. Sinha, *J. Sci. Instrum.* **42**, 696 (1965).
6. A. M. Glazer, P. Groves, and D. T. Smith, *J. Phys. E: Sci. Instrum.* **17**, 95 (1984).
7. E. D. Dias, R. Pragasaam, V. R. K. Murthy, and B. Viswanathan, *Rev. Sci. Instrum.* **65**(9), 3025 (1994).
8. René Meyer, Rainer Waser, Klaus Prume, Torsten Schmitz, and Stephan Tiedke, *Appl. Phys. Lett.* **86**, 142907 (2005).
9. T. Fukami, H. Yanagisawa, and H. Tsuchiya, *Rev. Sci. Instrum.* **54** (11), (November 1983).